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10/520,314	01/05/2005	Joost Maarten Zitzmann	NL 020593	2573

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EXAMINER	
LIN, PHYOWAI	

ART UNIT	PAPER NUMBER
2613	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

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Office Action Summary	Application No.	Applicant(s)	
	10/520,314	ZITZMANN ET AL.	
	Examiner	Art Unit	
	PHYOWAI LIN	2613	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7 and 10-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-7 and 10* is/are allowed.

6)☒ Claim(s) *11-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Amendments to the specification filed on November 30, 2007 have been fully considered and accepted by Examiner.

Drawings

2. Amendments to the drawing filed on November 30, 2007 have been fully considered and accepted by Examiner.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

4. **Claim 11** is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

5. **Claim 11** recites the limitation "the optical converter circuit" in line 2. There is insufficient antecedent basis for this limitation in the claim.

For examination on the merits, the recited limitation will be read as----an optical converter circuit----.

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 11,12,14,16 and 17** are rejected under 35 U.S.C. 103(a) as being unpatentable over Imajo (US Pub Number 2002/0122233) in view of Weigand (US Patent Number 6489856) and Harford (US Patent Number 5898347).

Regarding to claim 11, Imajo discloses an optical receiver circuit (see FIG.9) comprising:

an attenuator circuit (electronic attenuator 22) connected to the optical converter circuit (light receiving circuit with a light receiving diode 10), the attenuator circuit to receive an electrical signal from an optical converter circuit and to provide a constant output signal level of the optical receiver circuit (see paragraph [0111] and FIG.9). Additionally, Imajo disclose an attenuation circuit attenuates an electrical signal from the optical converter circuit dependent on a characteristic value of the electrical power output by a sensor circuit (see paragraph [0118] lines 1-5; paragraph [0113] lines 1-3; paragraph [0111] lines 6-14 and FIG.9 where in a sensor circuit (from point B to CPU 24 functioning like sensor circuit part) outputs the voltage at point B and couples into CPU 24 performing the gain control voltage value for controlling the gain in the electronic

attenuator 22 and so that the attenuator 22 can attenuate the electrical signal from the optical converter circuit into desired level).

Even though Imajo discloses the attenuator circuit connects to the optical converter circuit, and receives the gain control voltage value from sensor circuit for controlling the gain in the attenuator circuit, Imajo fails to specifically disclose the attenuator circuit comprises a plurality of cascaded attenuator stages which can be selectively attenuated the signal and a capacitor connected between adjacent attenuator stages to separate the adjacent attenuator stages.

Weigand discloses attenuation circuit 15b, 22, 15a are formed in cascaded attenuator stages and if one of the bit control signals 14 and 16 is turned on to logic high, it can turn the one of the attenuator circuits 15b, 22, 15a to active state (see column 4, lines 4-49 and FIG.2).

Harford discloses a capacitor (C54) connected between adjacent attenuator stages to separate the adjacent attenuator stages (see column 3, lines 30--35 and FIG.1 where in the capacitor (C54) connects between adjacent attenuator stages 12 and attenuator stage 14).

Therefore, it would have been obvious to a person of ordinary skill in the art at the same time the invention was made to modify Imajo with the teaching of Weigand and Harford so as to implement a plurality of attenuator stages in cascaded form and capacitor between adjacent attenuator stages inside the attenuator circuit because it would allow the attenuation will be arithmetically additive provided return loss of each unit is extremely good in optical receiving circuit.

Regarding to claim 12, Imajo, Weigand and Harford disclose everything claimed as applied above (see claim 11). In addition, Imajo discloses the optical receiver circuit further comprising an input capacitor (capacitor 13-see FIG.9) to connect an input end of the attenuator circuit to an output of the optical receiver circuit (see FIG.9 where in capacitor 13 connects between the output of the optical receiving circuit and input end of the electronic attenuator 22).

Regarding to claim 14, Imajo, Weigand and Harford disclose everything claimed as applied above (see claim 11). In addition, Imajo discloses the attenuation stage is connected in parallel with the optical converter circuit (see FIG.9).

Weigand disclose wherein each attenuator stage further comprising: a resistor (resistor R3); and a semiconductor switch (FET Q3) in series with the resistor (see column 3, lines 58-62 and FIG.2).

Therefore, it would have been obvious to a person of ordinary skill in the art at the same time the invention was made to modify Imajo with the teaching of Weigand and Harford so as to implement a plurality of attenuator stages in cascaded form and capacitor between adjacent attenuator stages inside the attenuator circuit because it would allow the attenuation will be arithmetically additive provided return loss of each unit is extremely good in optical receiving circuit.

Regarding to claim 16, Imajo, Weigand and Harford disclose everything claimed as applied above (see claim 11). In addition, Imajo discloses the optical receiver circuit further comprising the optical converter circuit connected to an attenuator circuit, the

optical converter circuit to convert optical power into the electrical power (see paragraph [0111] lines 1-5 and FIG.9).

Regarding to claim 17, Imajo, Weigand and Harford disclose everything claimed as applied above (see claim 11). In addition, Imajo discloses the optical receiver circuit further comprising the sensor circuit connected to the optical converter circuit, the sensor circuit to detect and output the characteristic value of the electrical power (see paragraph [0118], lines 1-5 and FIG.9 where in from point B to CPU 24 functioning like sensor circuit part which connects to the light receiving diode 10 and can detect and output the value of the electrical power).

8. **Claim 13** is rejected under 35 U.S.C. 103(a) as being unpatentable over Imajo (US Pub Number 2002/0122233) in view of Weigand (US Patent Number 6489856) and Harford (US Patent Number 5898347) as applied to claim 11, respectively, above, and further in view of Skrobko et al. (US Pub Number 2003/0090320).

Regarding to claim 13, Imajo, Weigand and Harford disclose everything claimed as applied above (see claim 11). In addition, Harford discloses the optical receiver circuit further comprising an output capacitor connects an output of the attenuator circuit (see column 3, lines 30--35 and FIG.1 where in the output capacitor connects after the output of the attenuator stage 16 (after transistor Q7)).

Skrobko et al. discloses a tilt network 130 which includes attenuator and capacitor stages inside and the output of the tilt network 130 couples into the transformer 135 (matching network) for matching the RF signal to two post amplifiers 140 and 150 (see paragraph [0019] lines 9-11; paragraph [0022] lines 7-9 and FIG.1).

Therefore, it would have been obvious to a person of ordinary skill in the art at the same time the invention was made to modify Imajo with the teaching of Weigand and Harford so as to implement an output capacitor of the attenuator circuit to the input of a matching circuit inside the optical receiver circuit because it would allow the optical receiver circuit achieving desired matching signal level that can be used with another optical devices for making optimal optical receiving signal.

9. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Imajo (US Pub Number 2002/0122233) in view of Weigand (US Patent Number 6489856) and Harford (US Patent Number 5898347) as applied to claim 14, respectively, above, and further in view of Kasashima et al. (US Patent Number 5694069).

Regarding to claim 15, Imajo, Weigand and Harford disclose everything claimed as applied above (see claim 14). However, they fail to specifically disclose wherein each attenuator stage further comprises: another resistor, wherein the resistors are connected in series; and another semiconductor switch connected in parallel with the other resistor to bridge the other resistor.

Kasashima et al. disclose in the optical receiving circuit having another resistor (resistor 14), wherein the resistors are connected in series; and another semiconductor switch (FET switch 12) connected in parallel with the other resistor to bridge the other resistor (see FIG.1 where in resistors 13 and 14 are connected in series and also connected with FET switch 11 in series and one of the resistors 13 is connected in

parallel with FET switch 12 and one of the resistor 14 is being bridged by FET switch 12).

Therefore, it would have been obvious to a person of ordinary skill in the art at the same time the invention was made to modify Imajo, Weigand and Harford with the teaching of Kasashima et al. so as to use two resistors with one semiconductor switch in series and one of the resistor is being bridged to another semiconductor switch in optical receiving circuit because it would allow the optical receiving circuit having low power consumption and high switching states by using semiconductor FET switch.

10. **Claims 18 and 19** are rejected under 35 U.S.C. 103(a) as being unpatentable over Imajo (US Pub Number 2002/0122233) in view of Weigand (US Patent Number 6489856) and Harford (US Patent Number 5898347) as applied to claim 17, respectively, above, and further in view of Farmer et al. (US Pub Number 2004/0253003).

Regarding to claim 18, Imajo, Weigand and Harford disclose everything claimed as applied above (see claim 17). In addition, Imajo discloses where in the sensor circuit comprises a resistor network (resistor 11) connected to the optical converter circuit, the resistor network derives a control voltage VCONTR from the electrical power as the characteristic value of the electrical power (see paragraph [0118], lines 1-5; paragraph [0111], lines 6-10 and FIG.9 where in a resistor 11 connects in series with light receiving diode 10 and from point B derives a received light voltage value and then the received light voltage value couples to CPU 24 in order to derive output control voltage).

However, Imajo fails to specially disclose another resistor from resistor network, which connects to the light receiving diode 10.

Farmer et al. in the same field of endeavor disclose optical receiving circuit having resistor network (resistor 340 and resistor 410), which connect to the light receiving diode 117 (see paragraph [0089], lines 14-22 and FIG. 4).

Therefore, it would have been obvious to a person of ordinary skill in the art at the same time the invention was made to modify Imajo, Weigand and Harford with the teaching of Farmer et al. so as to use decoupling resistor 410 (part of resistor network) in optical receiving circuit because it would allow the optical receiving circuit having decoupling resistor 410 for preventing modulated current flow into the gain controller (control voltage)).

Regarding to claim 19, Imajo, Weigand, McGillan and Farmer et al. disclose everything claimed as applied above (see claim 18). In addition, Imajo discloses the optical receiver circuit includes A/D converters 25 after the CPU circuit for converting the control voltage signal from analog state to digital state (see FIG.9).

Weigand disclose the optical receiving circuit further includes: wherein the respective attenuator stages each have a different attenuation value (see column 4,lines 4-49 and FIG.2 where in any appropriate resistance value can change the attenuation level of step attenuator circuits15b, 22, 15a so that each step attenuator circuit can have a different attenuation value).

Therefore, it would have been obvious to a person of ordinary skill in the art at the same time the invention was made to modify Imajo, Weigand and McGillan with the

teaching of Farmer et al. so as to use decoupling resistor 410 (part of resistor network) in optical receiving circuit because it would allow the optical receiving circuit having decoupling resistor 410 for preventing modulated current flow into the gain controller (control voltage)).

Allowable Subject Matter

11. **Claims 1-7 and 10** are allowed.

12. The following is an examiner's statement of reasons for allowance:

Claim 1 is allowed because the closest prior art, Imajo (US Pub Number 2002/0122233) fails to anticipate or teach wherein the attenuator circuit comprises a step attenuator circuit comprising: a plurality of cascaded attenuator stages, wherein each of the continuing stages comprises two resistors and a semiconductor switch in series resistors and another semiconductor switch connected to bridge one or resistors; and capacitors to separate respective input ends the attenuator stages, and input capacitor to connect an input end of the attenuator stages to an output of the optical receiver circuit, and an output capacitor to connect an output of the attenuator circuit to a load impedance.

Imajo simply discloses the optical receiving circuit includes an optical converting circuit, a sensor circuit, an attenuator circuit and based on electrical control signal from the sensor circuit, the attenuator circuit is configured to provide a constant output signal level of the optical receiving circuit.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to PHYOWAI LIN whose telephone number is (571) 270-1659. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kenneth Vanderpuye can be reached on (571) 272-3078. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

PWL

02/08/08

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SUPERVISORY PATENT EXAMINE